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Effect of surface condition on boiling heat transfer from silicon chip with submicron-scale roughness

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Abstract

Boiling heat transfer on treated silicon surfaces was studied. Experiments were conducted to investigate the effects of submicron-scale roughness on the boiling heat transfer at a subcooled condition in FC-72 at the ambient pressure. Two-type of treated silicon surfaces were prepared for boiling surfaces using anodisation with HF (hydrofluoric acid) based electrolyte and DMF (dimethylforamide) based one. The back side of the treated surface was glued to the back side of the other silicon chip on which thin film heaters and thin film temperature sensors were fabricated using conventional MUPs processes with doped polysilicon. The treated chips with submicron-scale roughness which provide many possible nucleation sites showed considerable enhancement in the nucleate boiling heat transfer coefficients compared to the untreated silicon surface. Further, the critical heat flux (CHF) of the treated surfaces increase linearly to the increase in the effective area for boiling.

Keywords: CHF (critical heat flux); Nucleate boiling; Silicon surface; Submicron-scale roughness

1. Introduction

Direct immersion cooling [1] has been considered as one of the promising methods to cool high power density chips. A fluorocarbon liquid such as FC-72 is a prime candidate for direct immersion cooling since it is chemically and electrically (high dielectric strength) compatible with microelectronic components [2]. However, this liquid having appropriate boiling point of 56 °C at 1 atm for use of the immersion cooling method possesses poor thermal transfer properties compared to the common fluids such as water. This dielectric liquid, especially, shows high wetting behavior that causes it to have unusually high incipient boiling superheat [3]. Further, boiling in dielectric fluids is characterized by its relatively small value of the critical heat flux (CHF) with plain tube, which is about 10 W/cm^2 [4].

A number of studies have been done to enhance the boiling heat transfer coefficients at the nucleate boiling region with help of artificially formed nucleation sites on the boiling surfaces. The surface treatment techniques developed to provide high density nucleation sites are categorized as structured surfaces [5] such as Gewa-T surface [4], porous metal coating [6–8] and chemical etching with open surface [9]. Of these, the porous metal coating [8] provided a significant decrease of incipient superheat and correspondingly significant enhancement of nucleate boiling heat transfer coefficient about 300% compared to the untreated surface. Such dramatical enhancement in the nucleate boiling heat transfer might be due to the vapor–liquid exchange and thin film nucleation inside the structure.

Many researchers have also been tried to enhance CHF or the maximum cooling limit by increasing the effective area of the boiling surface. Nakayama et al. [10] achieved the heat flux level of above 100 W/cm^2 with $\Delta T_{sat} = T_w - T_{sat}$ (wall superheat) $\cong$40 K in FC-72 by attaching studs covered with miniature fins to the surface of heat source. Using a square-shaped stud in a diamond configuration, Anderson and Mudawar [11] obtained a CHF as high as 63 W/cm^2 in FC-72. Very recently, Honda et al.

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Nomenclature

A	area [m^2]
h	convection heat transfer coefficient [W/m^2 K]
k	thermal conductivity [W/m K]
l	characteristic length for pin [m]
L	length [m]
T	temperature [K]
P	fin pitch [μm]
Q	heat transfer rate [W]
q''	heat flux [W/m^2]

Subscripts

c	characteristic
chip	chip
s	surface
sat	saturated
Si	silicon
sub	substrate
TCR	thermally conductive RTV (room temperature vulcanising)
w	wall
∞	environmental condition

[12] have obtained a considerable heat transfer enhancement at the nucleate boiling region and 230% increase in the CHF from the micro-pin-finned chip with submicron-scale roughness. Further the CHF as much as 120 W/cm^2 in FC-72 was obtained by increasing the effective area for boiling region using a heat spreader [13].

In this study, two kinds of treated surfaces with submicron-scale roughness were tested at a subcooling condition in FC-72. The treated surfaces tested in this study are typical open surfaces which function differently to the nucleate boiling from the structured surfaces [4–8]. One of the treated surfaces has relatively small number of possible nucleation sites that is about $10^6/cm^2$ and 3% increase in the effective boiling area. The other one has large number of possible nucleation sites that is about $10^8/cm^2$ and 52% increase in boiling area. Careful attention was paid on the measurement of the base temperature of the boiling surface in this study.

2. Boiling surface preparation and test chip fabrication

2.1. Boiling surface preparation

The treated silicon surfaces were prepared by the method of anodisation in dimethylforamide (DMF) based electrolyte (DMF:HF:H_2O = 92:4:4) and hydrofluoro acid based one (HF:H_2O:ethanol = 20:20:40) for 25 min under direct current (DC) density of 20 mA/cm^2 using P-type silicon wafer. The most important parameter of the electrolyte is its ability to supply oxygen and hydrogen. Oxygen is necessary for smoothing the pore tips and hydrogen is the decisive factor for the anisotropic growth and the passivation of micropore side walls [14]. The ethanol content in the electrolyte affects both the solution's ability to wet the hydrophobic porous silicon surface and the viscosity of the diffusion layer adjacent to the surface [15]. The conventional experimental apparatus of the anodisation was explained in detail by Halimaoui [16].

The AFM (atomic force microscope) images of the treated surfaces and a untreated silicon surface are shown in Fig. 1. The treated surface in the hydrofluoro acid based electrolyte has the root-mean-square (RMS) roughness of 307 nm with the maximum height of 1.56 μm. The treated surface which is denoted as PSHF brings 52% increase in the surface area for boiling and large number of possible nucleation sites formed between the irregular matrices of protrusions. On the other hand, the treated surface in the DMF based electrolyte has the RMS roughness of 163 nm with the maximum height of 0.61 μm. This treated surface which is denoted as PSDMF brings only 3% increase in the surface area for boiling and 3 or 4 possible nucleation sites of micro dimples per 20×20 μm^2.

2.2. Experimental chip fabrication

Polysilicon thin film heaters and temperature sensors were used in many MEMS (microelectromechanical systems) studies [17,18]. The silicon substrate on which heaters and sensors were fabricated is the same type of silicon wafer used in the treated surfaces. The two serpentine type polysilicon heaters for heating the test chip were fabricated on the silicon dioxide layer, and five polysilicon-temperature sensors were fabricated between the two heaters as shown in Fig. 2(a). The back side of the treated wafer was attached to the other side of the silicon substrate of heaters and sensors using TCR (thermally conductive RTV; $k_{TCR} = 2$ W/mK). The bonded test chip was inserted into PCB (printed circuit board) and was connected to electrical equipments using wire ball bonding. Finally, the model chip was insulated thermally by using the resin epoxy and silicone rubber as shown in Fig. 2(b).

3. Experimental apparatus and procedures

3.1. Experimental apparatus

A typical pool boiling vessel utilized in this experiment is shown in Fig. 3. The main components of the test facility used are measurement and control system. The boiling ves-

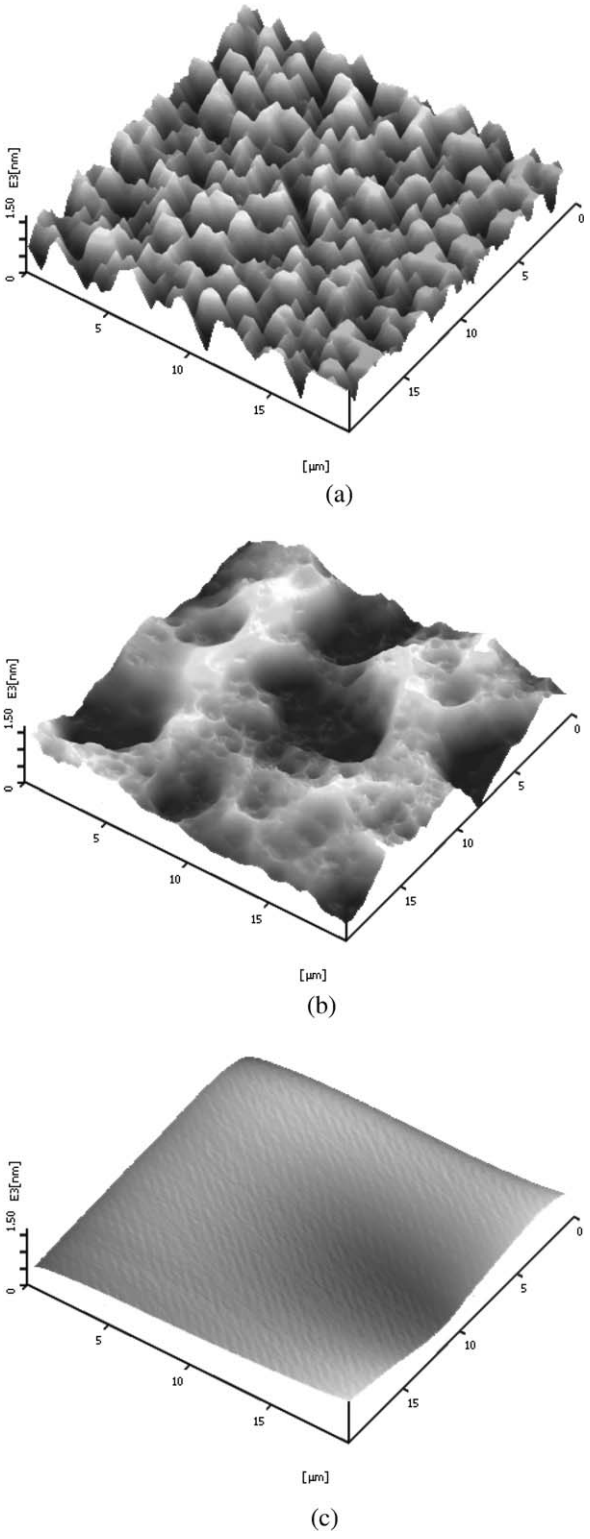

Fig. 1. AFM image of chip surface. (a) PSHF, (b) PSDMF and (c) SiBare.

sel with dimension of 160 mm × 160 mm × 500 mm was made of stainless steel. Quartz sight glass windows to facilitate visual observing were made on the front and rear walls of the vessel with brass flanges. The top cover of the vessel made of stainless steel has taps for thermocouple connectors, cooling water loops, electric cables, and vent for remaining ambient pressure. A fluorinert FC-72 used as working fluid was heated by four cartridge heaters imbedded in the brass plate attaching to the bottom of the test chamber. Heat was removed from the vessel via a water cooled condenser coiled within the upper section of the vessel. The bulk fluid temperature was measured by two K-type thermocouples located above the test chip. A temperature controller (OMEGA, E924K29) powered the cartridge heater to maintain the liquid temperature. The pressure inside the vessel of 1 atm was maintained by controlling the cold water stream through the condenser.

3.2. Sensor calibration

Although the polysilicon line heater fabricated on SiO_2 layer is a good sensor to measure the temperature [17,18], the resistance values from the sensors may be different depending on the degree of phosphorus doping, the sensor dimensions fabricated and the condition of wire bonding. Thus, all the temperature sensors were calibrated before measurements. To obtain a calibration curve between the temperature and electric resistance of the temperature sensors on the chip, non-insulated test chip was immersed in a pool of FC-40. The temperature of the chamber filled with FC-40 was controlled by heaters. The temperature of the working fluid was controlled by a temperature controller with K-type thermocouples located near the bottom, center and near the top of the chamber. After the thermocouples indicated stable value within ±0.5 °C then the resistance of sensor was measured in the temperature range between 50 °C and 149 °C, near the boiling temperature of FC-40. These temperature-resistance data for the temperature sensor were tabulated and curve fitted.

3.3. Experimental procedure

The test chip was placed on the aluminum plate flatly using a leveling instrument. A digital camcorder was aligned with quartz window for observing the boiling phenomena on the treated surfaces. Temperature of working fluid in the vessel was maintained about 22 ± 1.5 °C by using the temperature controller and by circulating water during the experiments. Heat was supplied by controlling the input voltage to the heaters. Any degassing procedure for the test liquid was not done in this experiment because the boiling curves and the values of the critical heat flux are closed to the case of degassed FC-72 [12]. Experimental results were obtained by averaging the five experimental data sets and the maximum deviation during the repetition was found to be about ±2 °C.

3.4. Error analysis

The heat flux was calculated by using the following equation by assuming that uniform heat generates in the silicon wafer:

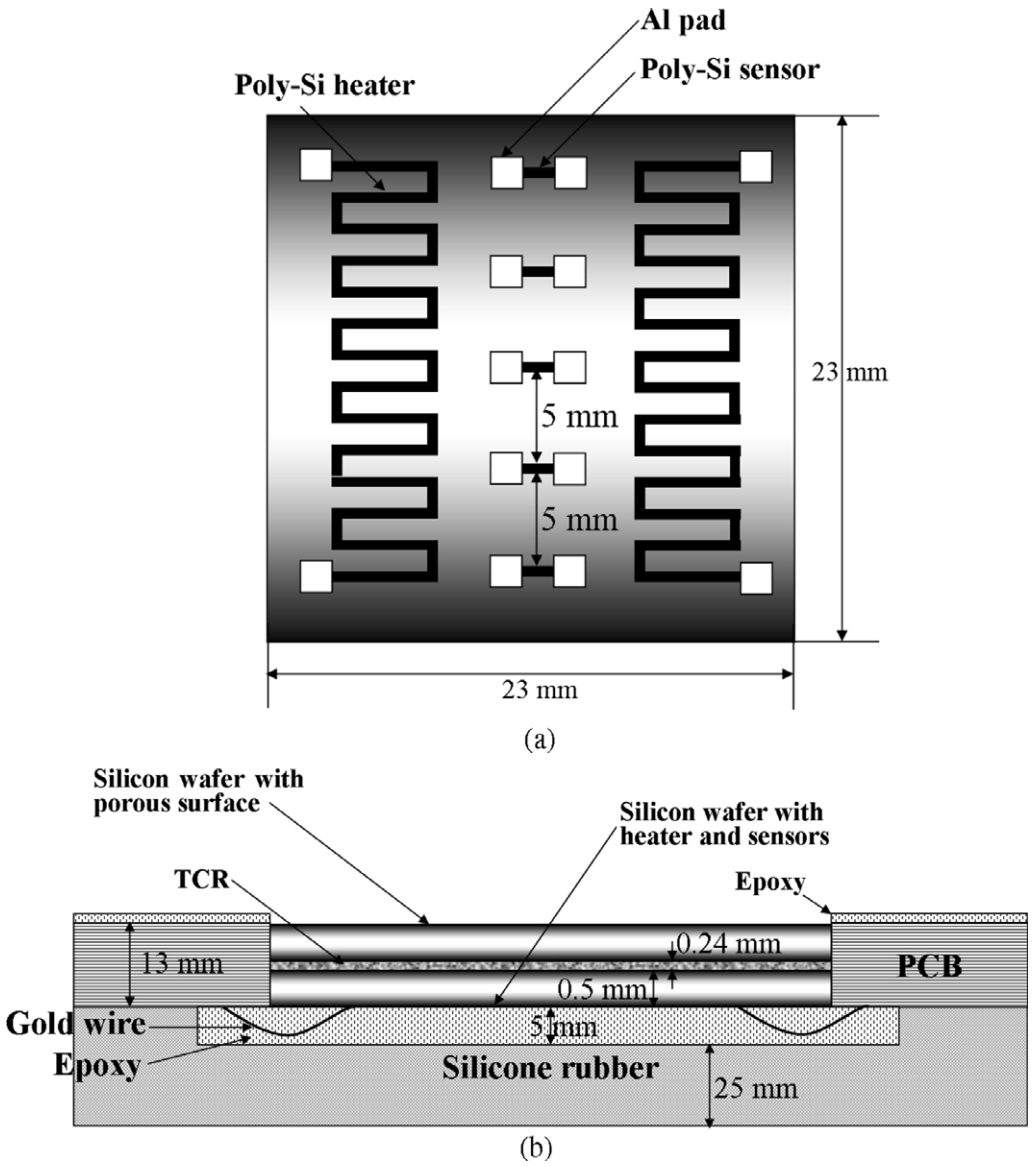

Fig. 2. Schematics of chip for boiling experiment. (a) Fabricated heaters and sensors, (b) cross-sectional view of experimental chip.

$$q'' = Q_{\text{chip}}/A_{\text{chip}} \tag{1}$$

Q_{chip} in Eq. (1) is equal to the voltage times the current to the chip. The voltage to the chip was measured by a digital voltmeter, which is accurate within the range of ±0.05 V. The current to the chip was determined by measuring the voltage drop across a resistor connected with a series of chips. The accuracy of the current measured is less than ±0.005 A so that the estimated uncertainty in the heat flux is about ±1.25% at low powers and ±1.02% at high powers with accounting for the error in the measurement of the chip surface area below ±1.0%. The error in the measurement of the wall temperature by using the polysilicon sensors is about ±0.5 K and the error in the measurement of the liquid temperature by the K-type thermocouples is also about ±0.5 K so that the estimated experimental errors for heat transfer coefficient are about 4.4% at the lowest heat flux and 3.9% at the highest one.

4. Experimental results and discussion

Fig. 4 shows the variation of measured liquid and wall temperature depending on the heat flux applied to the chip. The wall temperature of the chip was estimated using the following equation:

$$T_{\text{w}} = T_{\text{s}} - q''\left(\frac{L_{\text{TCR}}}{k_{\text{TCR}}} + \frac{L_{\text{Si}}}{k_{\text{Si}}}\right) \tag{2}$$

where T_{s} is the measured temperatures by the polysilicon sensors and the thickness of L_{TCR} was measured by microscope with a reference scale. As shown in Fig. 4, the local liquid temperature at the chip level maintains its temperature within ±1.5 K during the experiment. The temperature measured at the center of the chip increases linearly with increase in the heat flux. On the other hand, the temperature measured at 10 mm from the center does not increase

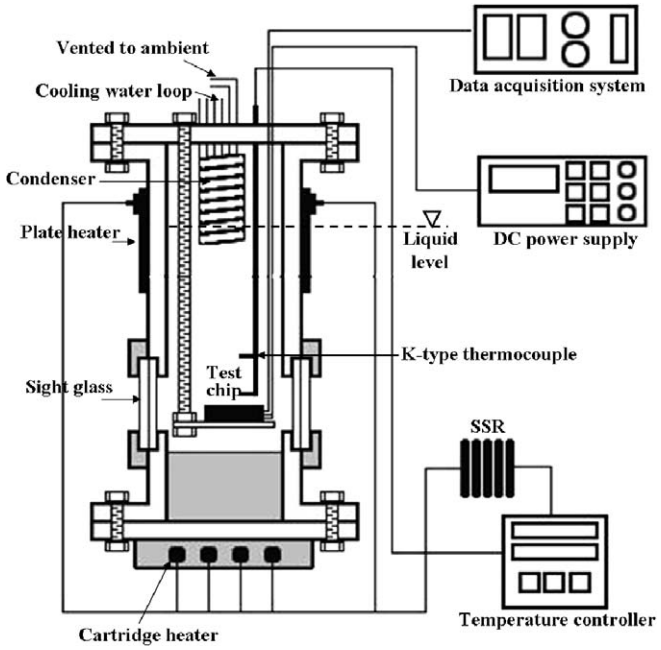

Fig. 3. Schematic of experimental apparatus.

above the heat flux of 5 W/cm^2. This observation is somewhat different from that of Honda et al. [12]. In their 1 mm × 1 mm heater, the increasing trend in the temperature measured at the rim of the heater just follows the center temperature. The maximum difference between the temperatures measured at the center and near the rim of the boiling surface is about 20 K. In this study, the wall temperature was taken as the average temperature of the measured temperatures at five points, which is closed to the temperature measured at 5 mm from the center. In the micro hot plate designed in this fashion, the lateral distribution of temperature is expected to be more uniform except the edge. Fig. 5 shows the estimated values by Eq. (2) and measured ones by a thermocouple at the center of chip depending on the heat flux for a smooth surface of silicon wafer. In this particular test, the thermocouple attached to the center of the chip was covered by silicone on which no boiling occurred. The maximum deviation between those values is less than ±3 °C. It is noted that the heat loss from the heater through epoxy resin and silicone rubber having thermal conductivity of 0.033 W/m K at room temperature is estimated to be about 0.03 W/cm^2 at the heat flux of 17 W/cm^2 so that it is negligible.

For microstructured surfaces, it is quite difficult to define the wall temperature, which is very important to estimate the wall superheat [19]. In fact, as shown in Fig. 6, computer calculation of the temperature distribution of the chip surface provides two hot regions above the heater. So, it is very hard to estimate temperature of the boiling surface by measuring the temperatures at the points along the line bisecting the two regions. In this calculation, convective boundary condition was used for the boiling surface and no heat transfer was assumed through the insulating layer. Fig. 7 shows comparison of the measured temperatures to the calculated ones at selected points. The difference between the measured and calculated temperatures at those points is as much as 3.9 °C at the heat flux of 20 W/cm^2. However, the calculated average temperature depending on the applied heat flux are in close agreement with the five points average data measured, which validates our method of estimating average surface temperature for the boiling surface.

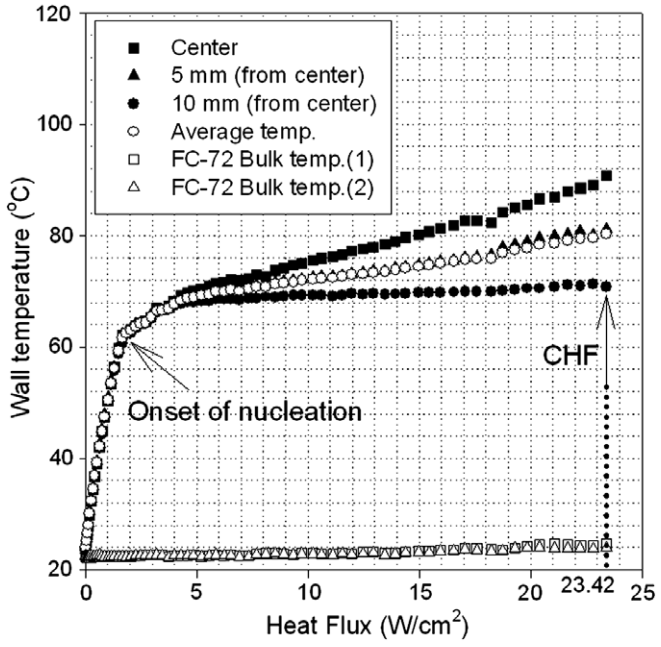

Fig. 4. Variation of measured wall and liquid temperature with heat fluxes.

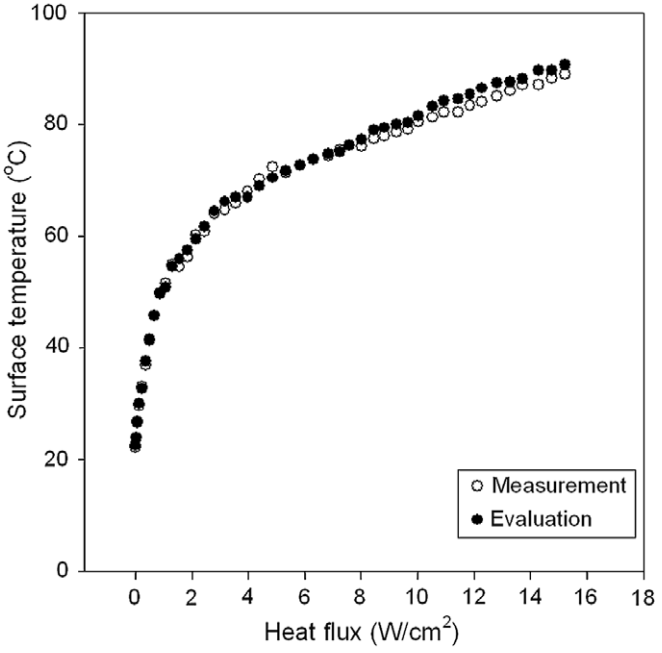

Fig. 5. Estimated and measured surface temperature at the center of the bare silicon chip.

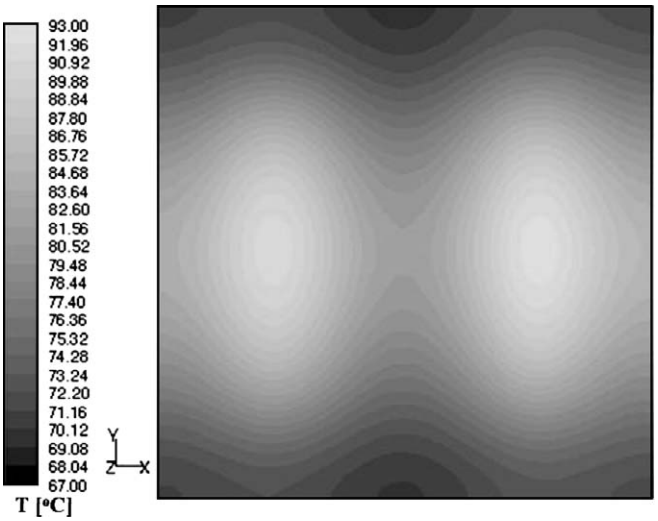

Fig. 6. Calculated temperature distribution on the chip surface at the heat flux of 20 W/cm^2.

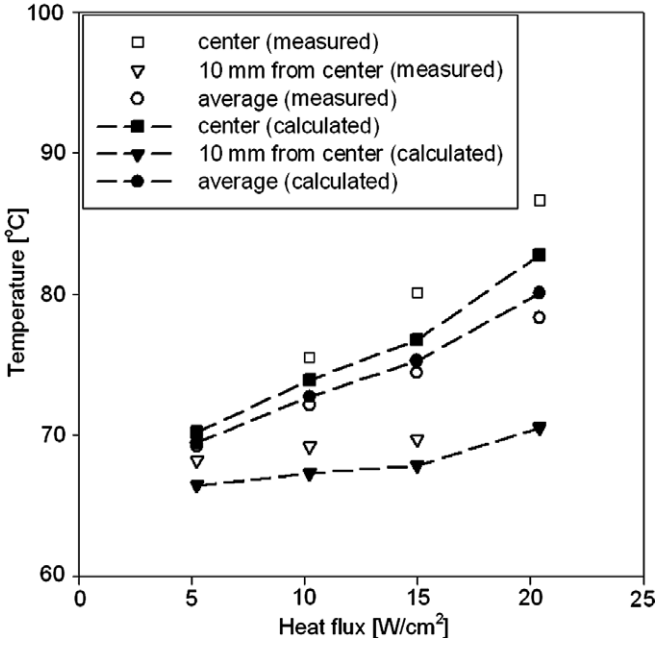

Fig. 7. Calculated and measured temperatures at selected points and calculated and measured average temperatures of the chip surface.

Fig. 8 shows the boiling curves for all tested chips immersed in FC-72 at a subcooling of 34 K because the heat transfer characteristics in the nucleate boiling region at the subcooling condition is essentially the same as the case of saturated condition except that the critical heat flux increases substantially at higher subcooling [12]. In the insert in Fig. 8, traditional log–log plot for the boiling curves are shown. For the smooth boiling surface, there is no abrupt transition between natural convection and nucleate boiling region. However, the point of onset of nucleate boiling (ONB) clearly appears for the treated surfaces. Rather modest temperature overshoot at ONB as shown in Fig. 8 leads to less significant boiling hysteresis. The slope in the boiling curve between ONB and CHF may be determined from the change in the bubble population density, as discussed by Honda et al. [12]. In this sense, Fig. 8 indicates that the active nucleation sites increases similarly for both PSHF and PSDMF surfaces as the surface temperature increases and more number of active nucleation sites are available at lower wall superheat for the PSHF surface.

Fig. 9 shows the corresponding heat transfer coefficients obtained from the heat flux data shown in Fig. 8 using the following relation:

$$h = q''/(T_w - T_\infty) \tag{3}$$

where T_∞ is liquid temperature. The measured heat transfer coefficient in natural convection region from the smooth silicon surface is about 150% higher than those from a well known correlation [20]. The maximum heat transfer coefficient at the CHF are about 2200–4000 W/m^2 K.

The ONB occurs at the wall superheat of 12 K for the PSHF chip and 17 K for the PSDMF chip, which indicates that the ONB on the boiling surface strongly depends on the number of nucleation site density. Of course, the incipient boiling occurs at lower temperature, 6.3 K for the PSHF surface and 7.6 K for PSDMF surface. The slope in the boiling curve from the PSHF chip is almost same as that from the PSDMF. However, the CHF achieved on the tested chips was found to be proportional to the increase in the effective area for boiling as clearly seen in Fig. 10. Note that the CHF value obtained from the smooth silicon surface is much greater than the CHF of 10 W/cm^2 obtained by Marto and Lepere without subcooling. In fact, for all the tested chips the CHF increase almost linearly as the degree of subcooling increases [12].

Effective surface area for boiling in the micro-pin-finned chip may be obtained by calculating the characteristic length scale for the pins considered. The characteristic length for the pin with constant cross section area is given by [21]

$$l_c = \left(\frac{k_{Si}A_c}{hP}\right)^{1/2} \tag{4}$$

With $k_{Si} = 80$ W/m K and h=16,000 W/m^2 K obtained at CHF [12], the characteristic lengths for the pins with thickness of 30 μm and 50 μm are 200 μm and 250 μm, respectively. For the effective boiling surface at the end of pin, the pin height is less than 10% of the characteristic length calculated by Eq. (4). If the pin height is greater than 0.1 l_c, a part of the extended surface will act as effective boiling surface with heat flux of the CHF, which was confirmed experimentally by Wei and Honda [19].

In Fig. 11, the boiling curves obtained from the treated surface of SiO_2 thin layer by sputtering and then dipping it into the mixture of HF, NH_4F and water for wet etching and from the smooth silicon surface of 1×1 cm^2 [12] and from the differenct sizes of diamond coated surfaces along

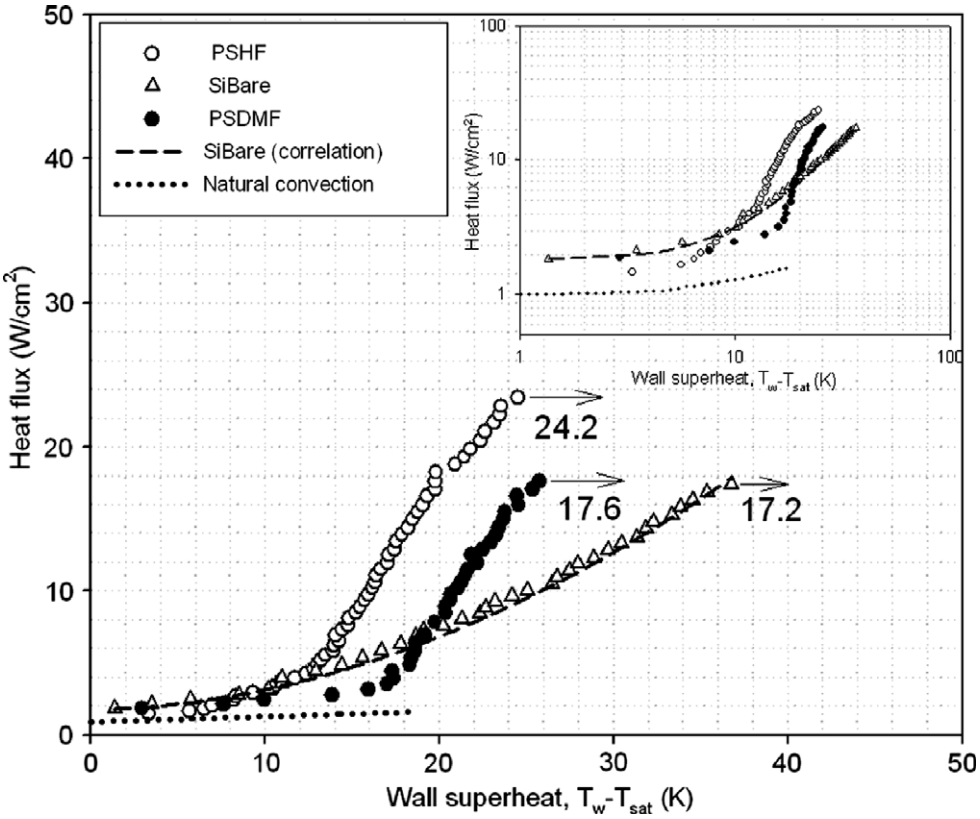

Fig. 8. Comparison of boiling curves at $\Delta T_{sub} = 34$ K.

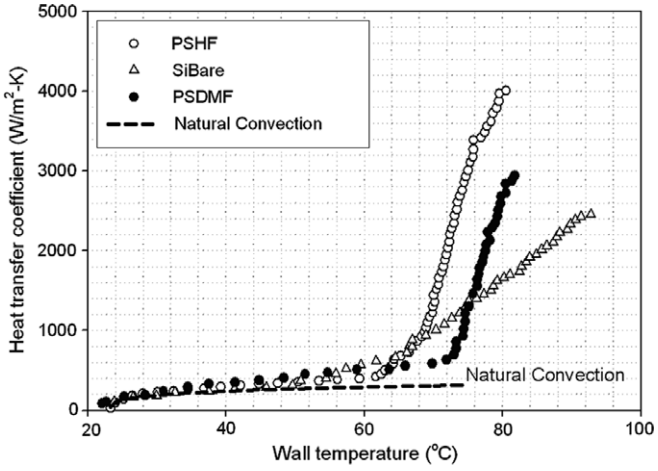

Fig. 9. Heat transfer coefficients from various surfaces tested.

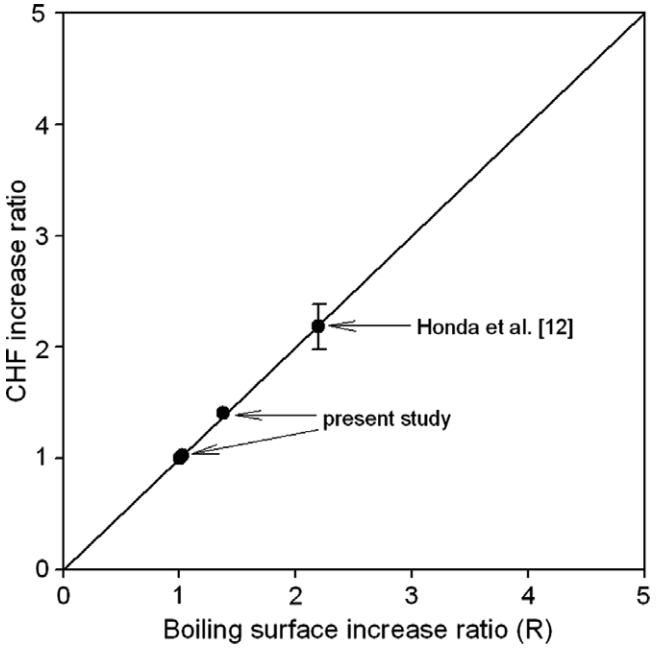

Fig. 10. Heat flux increase ratio vs. boiling surface increase ratio.

with our measured curves are presented. The treated surface by Honda et al. [12] has a very fine roughness with the RMS roughness of 32.4 nm and the maximum height of 0.27 μm, which are one order of magnitude smaller values compared to the treated surface of PSHF used in the present study. As can be seen in Fig. 11, there is no abrupt transition from the natural convection to nucleate boiling heat transfer regime for the smooth to fine roughness surface. For both smooth and treated surfaces, the CHF values obtained by Honda et al. [12] are 25% greater than the measured values in this study. This might be due to the fact that Honda et al. employed more larger heaters in their experiment. The effect of heater size on the CHF was also

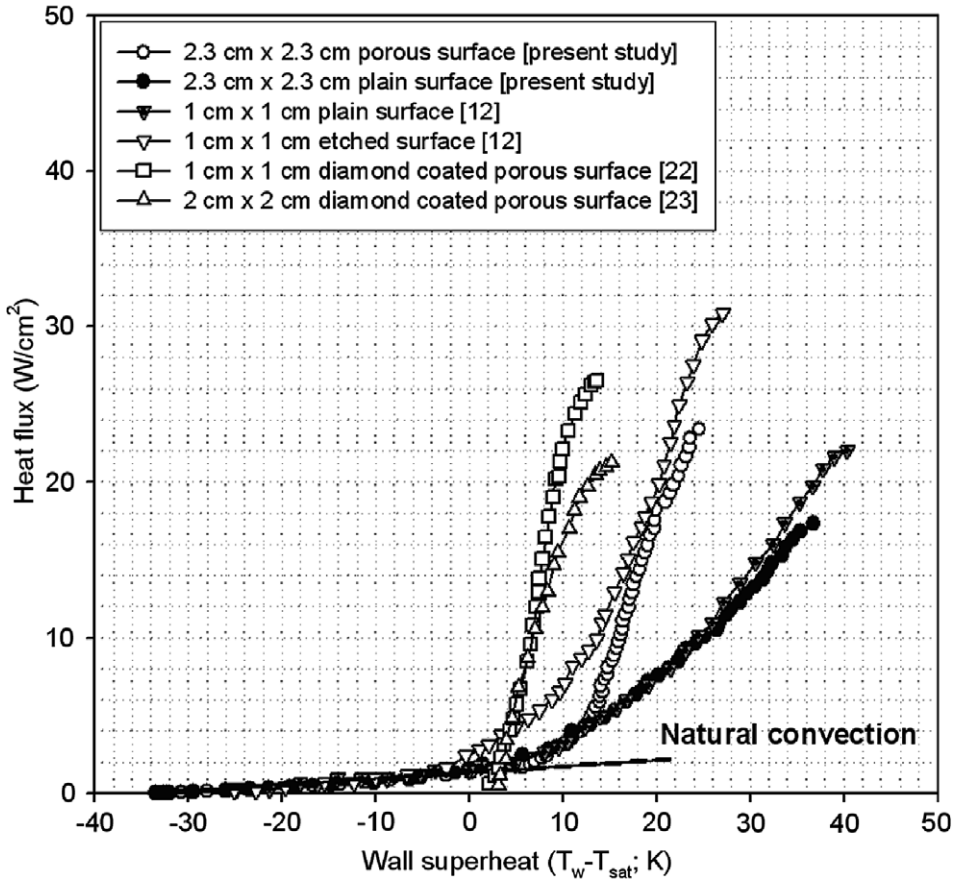

Fig. 11. Comparison of boiling curves obtained in this study with the ones by others [12,22,23].

confirmed experimentally for the diamond coated surfaces by Chang and You [22] and Rainey and You [23].

5. Conclusion

In this study, two kinds of treated surfaces with submicron-scale roughness were tested at a subcooling of about 34 K in FC-72. Surface temperatures of the test chip were obtained by polysilicon temperature sensors and uniform heat fluxes to the test chip were supplied by controlling the input voltage to the polysilicon thin film heaters precisely. One of the treated surfaces has relatively small number of possible nucleation sites that is about $10^6/cm^2$ and 3% increase in the effective boiling area. The other one has large number of possible nucleation sites that is about $10^8/cm^2$ and 52% increase in boiling area. There was no abrupt transition from the natural convection to nucleate boiling heat transfer regime for the smooth to fine roughness surface. The treated chips with submicron-scale roughness which may serve for nucleation sites as the surface temperature increases showed considerable enhancement in the nucleate boiling heat transfer coefficients. Furthermore, the critical heat flux (CHF) of the treated surfaces increases linearly to the increase in the effective area of boiling.

Acknowledgement

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